REMARKS

Applicant has made clarifying amendments to the preambles of claims 1 and 8. For instance, claim 1 was amended to call for "A superscalar, pipelined processor…" Applicant contends that it is not necessary to distinguish over the prior art to recite that "the processor implemented as a three way superscalar, pipelined architecture", as previously recited. Similar amendments have been made to claim 8.

The Examiner rejected Claims 1-38 under 35 U.S.C. §112, second paragraph, as indefinite. The examiner stated: "It is not clear whether micro-ops are meant to be microinstructions."

Applicant contends that the claims are definite. Applicant has amended the specification to clarify. As will discuss below, there is no indefiniteness in the claims.

As Applicant describes in the specification, "Typical microprocessor operations include adding, subtracting, comparing, and fetching operands from memory or registers. These operations result from execution a set of instructions that comprise a program."[1] Applicant also describes that: "The front end 16 fetches and decodes instructions into simple operations called micro-ops (μops)."[2] Applicant's specification also describes that: "The stack 100 is implemented in a microcode environment. This allows fast subroutine returns in microcode. It also allows fast assist returns in microcode."[3] Applicant also describes that: "The μIP stack 100 provides a mechanism for improving the performance of microcode (μcode) execution. Microcode is programming that is ordinarily not program-addressable but, unlike hardwired logic, is capable of being modified. Microcode may sometimes be installed or modified by a device's user by altering programmable read-only memory (PROM) or erasable programmable read-only memory (EPROM)."[4]

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[1] Page 1, lines 10-11
[2] Page 2, lines 17-19
[3] Page 5, lines 11-13
[4] Page 6, lines 3-9

Applicant contends that clearly there is not any confusion in Applicant's specification regarding the role of microcode, micro-ops and instructions. In summary, instructions are those elements that comprise a program, micro-ops are the result of decoding instructions, whereas microcode is not program addressable. It is generally used in assisting hardware to run.

Clarity is also found in Applicant's claims.

For example, claim 1 calls for: "… an out-of-order microinstruction pointer (μIP) stack for storing pointers in a microcode (μcode) execution core. Claim 1 thus is directed to microinstruction pointer (μIP) stack, not to microinstructions per se as the examiner seems to imply. Claim 1 also recites that the pointers are "associated with a common instruction that is decoded into a plurality of micro ops… ." That is, accordingly to claim 1, execution of the instruction and micro ops are assisted with microcode execution. However, the microinstruction pointer (μIP) is the name given to the element and that element has micro-instruction pointers (μIP) pushed onto or off of the microinstruction pointer stack, as described in Applicant's specification from page 12 to 25.

Accordingly, claim 1 and by analogy Claim 8 and Claim 32, each of which has analogous limitations as claim 1, and their respective dependent claims are also definite.

Accordingly, the claims are proper under 35 U.S.C. §112 and the rejection should be removed.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Respectfully submitted,

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Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

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